INITIAL TEST RESULTS OF SBRC-190, A MULTI-GAIN, CRYOGENIC READOUT MULTIPLEXER FOR IR DETECTOR ARRAYS

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ABSTRACT

SBRC-190 readout multiplexer – manufactured by Raytheon Infrared Operation – is a 1x32, multi-gain, capacitive transimpedance amplifier (CTIA) especially suitable for use with infrared detector arrays requiring low-bias levels – such as Ge:Ga far infrared detector arrays. The unit-cell design is based on the CRC-696 multiplexer which has been incorporated in SIRTF's MIPS instrument. In this presentation we will report on the results of the first set of tests conducted on several of these devices. We will discuss gain, uniformity, and read noise of the bare mux under correlated-double sampling at 4.2K.

Key words: readout, multiplexer, infrared, detector array, CTIA.

MULTIPLEXER DESIGN

The SBRC-190 readout is a 1x32, multi-gain, capacitive transimpedance amplifier (CTIA) designed for use with far infrared detector arrays. The unit-cell design is based on the CRC-696 multiplexer which has been incorporated in SIRTF's MIPS instrument. Several features were added to the basic CRC-696 unit-cell to improve the amplifier performance and flexibility. Figure 1 shows the basic schematic of this device.

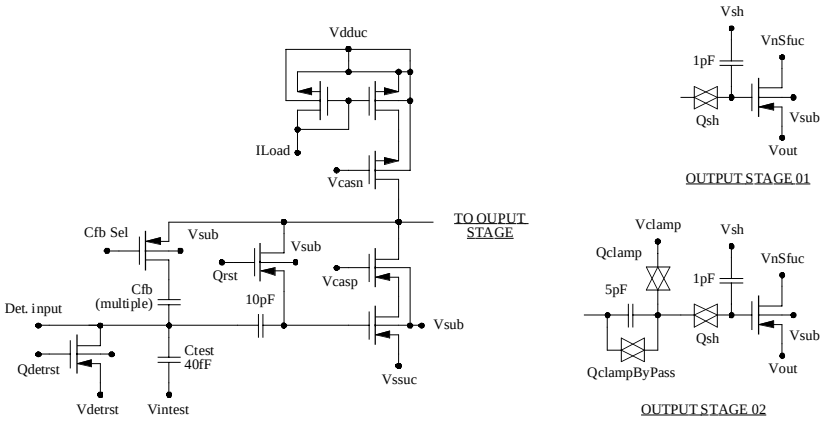

Fig. 1- Simplified schematic of the SBRC-190 readout multiplexer for both 01 and 02 types.

The amplifier employs the integration-reset scheme to convert the detector photo-current to a voltage that can subsequently be processed as needed. The front end is a pair of *p*-type MOSFETs in cascode configuration with eight capacitors in the feedback loop. The current to this signal cascode is provided by a current mirror – also in cascode configuration – comprised of *n*-type MOSFETs. The eight feedback capacitors may be enabled in sequence to provide different well capacities and, therefore, eight possible gain selections. During the integration time, where the reset switches are open, the photocurrent from the detector accumulates as an integrated charge on the feedback capacitor. By virtue of the negative feedback, the capacitor also pins the detector's input node to a constant voltage and, thereby, keeps the detector bias

constant regardless of the integrated signal. To improve channel-to-channel uniformity, the input is AC-coupled using a 10 pF capacitor.

Two types of devices were fabricated and designated as "01" and "02" depending on their output stages. "01" devices have a sample-and-hold circuit followed by a source-follower MOSFET. The sample-and-hold circuit can be disabled if desired. "02" devices add a clamp circuit before the sample-and-hold which can also be bypassed if desired. Both the clamp and sample-and-hold circuits are added to improve the sampling efficiency.

TEST SET UP AND THE DATA ACQUISITION SYSTEM

Raytheon Infrared Operation (RIO), the manufacturer of these devices, fabricated four lots, with various degrees of success, each having several wafers and many devices. The first two lots were severely out of specifications and, therefore, we did not test them. Lots 3 and 4 contained some devices that were functional according to manufacturer's probe tests, but neither one had devices that were within the parametric specifications. In particular, the MOSFET threshold voltages were outside the desired range.

As part of the initial tests, we tested several devices from Lot 3 and Lot 4. Each device was mounted in a 68-pin leadless chip carrier using epoxy. The output pads of the MUX were wire bonded to the chip-carrier pads but input pads were left floating. The chip carrier was held in a socket which, in turn, was mounted on a fanout board. There was direct thermal contact between the chip carrier and a cold finger through the hole in the chip socket. The fanout board was attached to the cold plate of a liquid-He dewar and shielded, stainless steel wires were used to connect the fanout board to the dewar connectors. The multiplexer bias and signal lines were bundled together, separate from the clock lines in order to minimize interference.

Our data acquisition system was specifically designed to drive SBRC-190 multiplexers, amplify and process the signals from the 32 MUX channels, and write the data to file for further processing. The analog and digital electronics were housed in separate enclosures with the analog box being attached directly to the dewar. We used a Power Macintosh G3 mini-tower as the host computer, and two National Instrument I/O boards for clocking and buffered A/D. The user interface was developed in LabVIEW.

TEST PROCEDURE AND SUMMARY OF RESULTS

The primary objective of our tests was to measure the unit-cell gain, the feedback capacitors, and the correlated-double-sampling (CDS) read noise for all 32 channels of the multiplexers at 4.2K. Except for minor adjustments, we used bias levels as recommended by the manufacturer and made no attempt to optimize the device performance by a systematic bias adjustment. The main objective for bias setting was to place the device in its operating range, and that generally meant adjusting the bias for the output FET. We also needed to adjust the Iload voltage to get the right current for the current mirror.

Many devices from both Lot 3 and Lot 4 were tested and, in general, they performed reasonably well. Some minor anomalies were observed which did not conclusively correlate to the lot or the wafer from which the device was selected. The MOSFET leakage at room temperature seemed to be too high and placed a limit on the usefulness of the room temperature tests. The difference between the devices from Lot 3 and Lot 4 were minor and are summarized below.

- The Lot 3 multiplexers had some non-operating channels, whereas all channels of the Lot 4 multiplexers were operating.
- The Lot 4 multiplexers had better uniformity across channels.
- Output FET gain for Lot 4 was slightly lower than Lot 3.
- The smallest signal capacitor for Lot 4 was larger than Lot 3, resulting in lower unit-cell gain.
- Read noise for both lots were comparable.
- For both lots, smaller signal capacitors had higher relative read-noise than larger capacitors.

Gain Tests at 4.2K

At 4.2K, the output FET gains as well as the unit-cell gains were measured for all channels. The bias levels were set to the nominal values as recommended by the manufacturer. The output FET gain was measured by opening the sample-and-hold switch, injecting a 100 mV RMS, 100 Hz sine wave into Vsh node, and monitoring the output. We observed reasonably consistent performance for all devices.

We measured the unit-cell gain for channels 1 through 32 and for all feedback capacitors. The tests were done by injecting a 100 mV RMS, 100 Hz sine wave into Vintest node and monitoring the output. Depending on the size of the selected feedback capacitor, the circuit offers different gain. A lock-in amplifier was used to measure the output signal more accurately, which was especially needed for the lower gain settings.

Using the output-FET gain and the unit-cell gain it is possible to calculate the values of the feedback capacitors. The Vintest node is coupled to the input of the unit cell through a nominal 40 fF capacitor (see Fig. 1). The unit-cell gain is the ratio of the 40 fF and the feedback capacitors multiplied by the output-FET gain. The main uncertainty in this calculation is the actual value of the 40 fF capacitor which cannot easily be measured.

Our measurements and calculations revealed a considerable difference between the actual and the designed values for the feedback capacitors. However, the difference seems to be reasonably consistent across all the devices tested. In particular, the smallest capacitor was almost twice as large as what it was designed to be. This difference is, primarily, attributed to the small but non-zero capacitance of the selecting MOSFET switches, which adds in parallel to the selected capacitor. The larger capacitors were measured to be much lower than what they were designed to be. The reason for this difference is believed to be the failing of some of the individual capacitors that in parallel form the aggregate large capacitors.

Figure 2 shows the output FET gain as well as the measured value of the smallest capacitor, Cfb0, for all channels of a typical device from Lot 4.

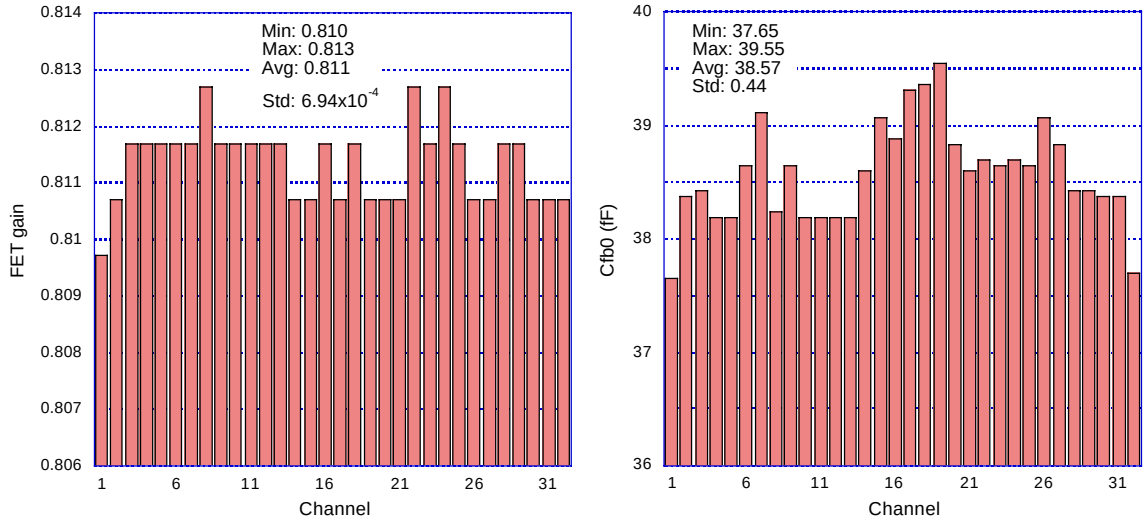

Fig. 2- Output FET gain (left) and the smallest feedback capacitor, Cfb0, (right) for all channels of a typical multiplexer at 4.2K.

CDS Read Noise at 4.2K

The noise measurements were done by running the multiplexer in the correlated-double-sampling mode at 100 Hz frame rate. The noise is the standard deviation of 1000 runs or integrations. There is a slight delay

between successive integrations when the data is transferred to the host computer during which the MUX is not clocking. This idle time did not seem to be long enough to cause thermal instability and additional noise. Thermal instability and MUX cooling, however, was observed when the idle time was increased indicating that clocking the MUX continuously or semi-continuously is a prerequisite for optimum performance. The noise measurements were repeated for all feedback capacitors and for all channels. As a base line, the read noise was also measured with both reset switches closed, which essentially shorted the input of the MUX.

With reset switches closed, the read noise scaled with the feedback capacitor as expected, indicating that the system is dominated by voltage noise. However, with the resets clocking, the read noise reached a limit of about 200 to 300 electrons for the five smallest capacitors. We believe there is an additional current noise component that is originated in the unit cell's current mirror circuit. For the largest capacitors, the voltage noise dominates the current noise component. Figure 3 shows the plots of the results for a typical device.

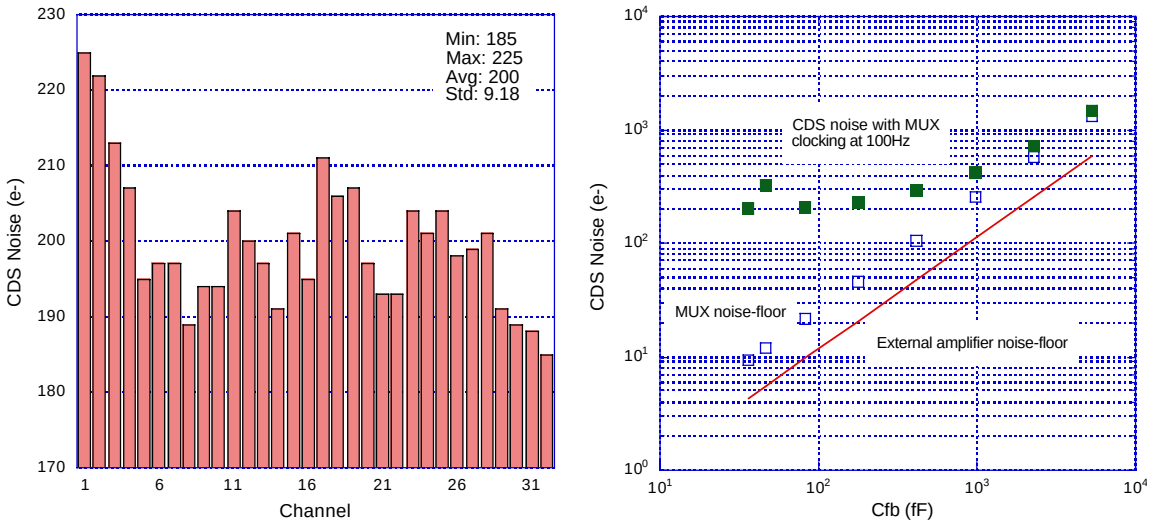

Fig. 3- CDS read noise of a typical MUX at 4.2K and 100 Hz frame rate. Left: The read noise for all channels with Cfb0 as the feedback capacitor. Right: The average read noise vs. feedback capacitors. The MUX noise-floor is the read noise with the reset switches closed, providing a reference baseline for the MUX. The MUX is current-noise limited at 200 electrons.

SUMMARY AND CONCLUSIONS

In summary, we have completed the initial tests of over twenty SBRC-190 bare readout multiplexers. Two of the four separate lots manufactured by Raytheon Infrared Operations had operational devices. However, the threshold voltages, even for the operational devices, were outside the specification range. Our test results indicated reasonable – although not optimum – performance. Lot 4 devices exhibited better operability. Some of the feedback capacitors deviated significantly from the designed values. The CDS read noise for lower capacitors were limited to about 200-300 electrons, well above the expected levels. Further testing and developmental work is underway.

ACKNOWLEDGEMENT

The authors wish to thank Nancy Lum of Raytheon, Ed Erickson of NASA-Ames Research Center, and Erick Young of University of Arizona for many insightful discussions on the subject. This work was performed at NASA-Ames Research Center, Sensors and Instrumentation Branch with the support of Craig McCreight as the Branch Chief.